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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,050	03/30/2004	Julie-Anne Francoise Marie Pruvost	550-515	1414

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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
SONG, JASMINE	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,050	PRUVOST ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *3-5,10,12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/30/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. The drawings filed on 03/30/2004 have been approved by the Examiner.

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 03/30/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

6. Claims 3-5,10 and 12-14 are objected to because of the following informalities:

In claims 3-5 and 12-14, lines 2-3, "memory access management unit" should be changed to – memory access control unit --.

In claim 5, last two lines, "...to, if said value is dirty, then to return said dirty data value to a main memory" should be changed to --, to return said dirty data value to a main memory if said value is dirty. --.

In claim 10, lines 6, "memeory" should be changed to – memory--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-2,6-11,15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by George et al., US 2004/0255176 A1.

Regarding claims 1 and 10, George teaches that an apparatus for processing data, said apparatus comprising:

a plurality of processor cores (Fig.7 system may include several processors of which only two processors are shown for clarity) operable to perform respective data processing operations (it is taught as processors 40 and 60 operable to perform read and write from system memory; section 0035, lines 1-2), at least two of said processor cores (it is taught as processors 40 and 60) being operable in a coherent multi-processing mode (it is taught as a processor need to cooperate in cache coherency schemes by responding to snoop requests when the processor is operating in a multi-processor system, section 0018, lines 1-3) sharing access to a coherent memory region (it is taught as each processor 40 and 60 shares accessing to the system memory 10, see Fig.7, processors 40,60 may be the processor 210 of Fig.2 and include caches 42,62, section 0034, lines 5-7); and

a memory access control unit (it is taught as a memory controller 34) coupled to said plurality of processor cores (Fig.7) and operable to perform coherency management operations (it is taught as the cache-coherency snoop requests initiated by a bus priority signal 226, section 0018, lines1-3 and section 0024, lines18-21) with respect to at least one cached copy of a data value from within said coherent memory region (George teaches the cache-coherency snoop requests, and snoop operation is

used to assure that any data written to system memory is accurately reflected in any matching cached copies); wherein

at least one of said processor cores operable in said coherent multi-processing mode is coupled to a cache memory (Fig.7), said cache memory being operable to remain active to service coherency management operations issued by said memory access control unit (it is taught as enough of the cache circuits and clocks are powered-on to respond to the cache coherency snoop request) whilst said processor core coupled to said cache memory is in an inactive power saving state (it is taught as the processor is operating in a low-power state such as the halt state or the stop grant state; section 0018).

Regarding claims 2 and 11, George further teaches that said processor core coupled to said cache memory is not clocked in said inactive power saving state (it is taught as the processor clock may be powered-down when a snoop request is received during the inactive power saving state such as halt state or the stop grant state, section 0018).

Regarding claims 6 and 15, George further teaches that in said inactive power saving state said processor core is responsive to a received interrupt signal to return to an active powered state (section 0032, lines 3 to last line).

Regarding claims 7 and 16, George further teaches that a wait for interrupt instruction executed by said apparatus triggers said processor core to enter said inactive power saving state (section 0016, lines 7-9, it is taught as a halt state may be entered by software executing a special MWAIT instruction) whilst said cache memory remains in said active state (section 0018, lines 8-10, it is taught as enough of the circuits and clocks are powered-on to respond to the cache-coherency snoop request).

Regarding claims 8 and 17, George further teaches that each of said processor core operable in said coherent multi-processing mode is coupled to a respective cache memory (Fig.7, section 0034, lines 5-7).

Regarding claims 9 and 18, George further teaches that said apparatus comprises an integrated circuit including said plurality of processor cores, said memory access control unit and said cache memory (it is taught as an integrated circuit includes processors 40, 60, caches 42,62, memory controller 34, bus bridge 32 in Fig.7; section 0034, lines 5-7 and 13-19).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable George et al, US 2004/0255176 A1, in view of Rowlands., US 6,993,631 B2.

Regarding claims 3 and 12, George teaches the claimed limitations as shown above (independent claims 1 and 10), George does not further teach that said cache memory is responsive to a copy coherency management request received from said memory access management unit to return a copy of a data value stored within said cache memory. However, Rowland teaches said cache memory is responsive to a copy coherency management request received from said memory access management unit to return a copy of a data value stored within said cache memory (it is taught as a remote node may begin the coherency process by requesting a copy of a cache block from the home node of that cache block using a coherency command; col.4, lines 1-13).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Rowlands into George's system such as said cache memory is responsive to a copy coherency management request received from said memory access management unit to return a copy of a data value stored within said cache memory because the copy coherency command can obtain the ownership of the cache block (col.3, lines 48-51 and col.4, lines 10-13 as taught by Rowlands) and memory coherency or consistency has been maintained (it is taught as a remote node begin the coherency process by requesting a copy of a cache block using a coherency command, col.4, lines 1-3 in Rowlands' reference).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated

one of ordinary skill in the art to implement the above combination for the advantages set forth above.

11. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable George et al, US 2004/0255176 A1, in view of Rowlands., US 6,993,631 B2 and Edirisooriya et al., US 2003/0195939 A1.

Regarding claims 4 and 13, George teaches the claimed limitations as shown above (independent claims 1 and 10), George does not further teach that said cache memory is responsive to a status change coherency management request received from said memory access management unit to change a status value associated with a data value stored within said cache memory. However, Rowlands teaches that said cache memory is responsive to a status change coherency management request received from said memory access management unit to change a status value associated with a data value stored within said cache memory (col.4, lines 13-20).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Rowlands into George's system such as said cache memory is responsive to a status change coherency management request received from said memory access management unit to change a status value associated with a data value stored within said cache memory because the state change coherency command can perform updates to cache lines or blocks within the caches and change the status of these updated cache lines or blocks within the caches as needed to maintain memory coherency or consistency (section 0016, lines 6-10 of Edirisooriya).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

12. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable George et al, US 2004/0255176 A1, in view of Sullivan., US 6,901,477 B2.

Regarding claims 5 and 14, George teaches the claimed limitations as shown above (independent claims 1 and 10), George does not further teach that said cache memory is responsive to a clean coherency management request received from said memory access management unit for a value stored within said cache memory to, if said value is dirty, then to return said dirty data value to a main memory. However, Sullivan teaches that said cache memory is responsive to a clean coherency management request received from said memory access management unit (col.6, lines 30-34) for a value stored within said cache memory (it is taught as the victim data stored within the disk cache; col.6, lines 34-36) to, if said value is dirty (col.6, lines 36-38 and Fig.4, step 76), then to return said dirty data value to a main memory (col.6, lines 38-39, it is taught as write the data back to the disk array, in this case, disk array is considered as main memory, also see background of the invention as taught in col.1, lines 21-44).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Sullivan into George's system such as said cache memory is responsive to a clean coherency management request received from said

memory access management unit for a value stored within said cache memory to return said dirty data value to a main memory if said value is dirty in order to maintain coherency between the memory subsystems (col.6, lines 66 to col.7, lines 8). In addition, the dirty data value has been written to the disk array (main memory) will releases the disk cache (cache memory) and makes it available for storing victim data, further increasing performance (col.7, lines 34-37).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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14. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

15. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

April 6, 2006

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100